國立中央大學96學年度碩士班考試入學試題卷

所別：電機工程學系碩士班 乙組(一般生) 科目：電子學
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1. 簡答與選擇題 (10 分)

1-1 Figure 1 shows a typical i_D - v_D characteristic of a p-n diode. As you can see, under forward-bias, we can use a small voltage swing to create a large current swing and obtain a transconductance (g_m) gain. This is the same as the case of i_C - V_{BE} characteristic (as shown in Figure 2) of a BJT, which can serve as an amplifier. Can you tell me why in nowadays we never use the diode to serve as an amplifier? (6 分)

1-2 In the early year (before the invention of transistor), the engineer still can use a diode to serve an amplifier. However, a circuit element is necessary to be integrated with the diode. Can you choose a suitable one from the following answers? (a) Resistor, (b) Capacitor, (c) Circulator, (d) Transformer. (4 分)

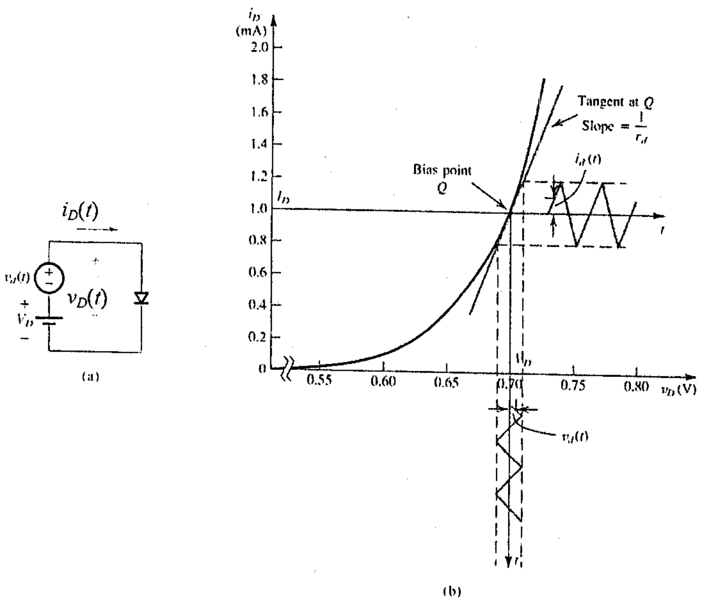

Fig. 1

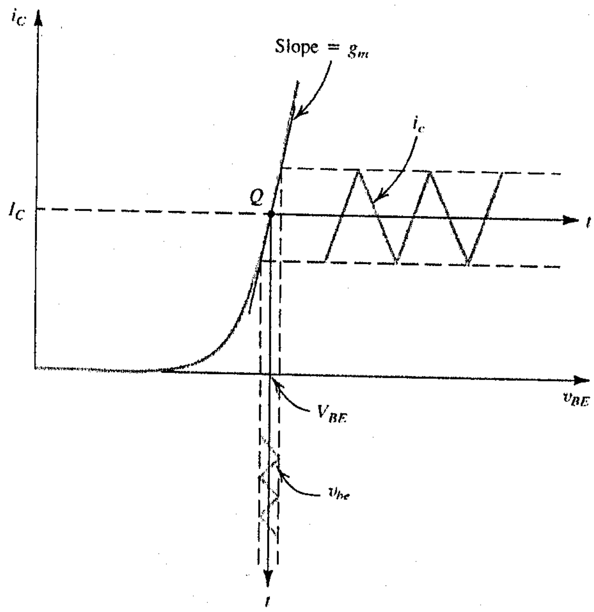

Fig. 2

2. 簡答與選擇題 (12 分)

Figure 3 shows a typical high-frequency small-signal model of a BJT.

2-1 Can you tell me, in order to achieve an **unilateral** amplifier, the value of which circuit element in this figure should be minimized? (a) r_π, (b) C_π, (c) g_m, (d) C_μ. (4 分)

2-2 The unit-gain cut-off frequency of a BJT, which can be obtained by the shown equivalent circuit model, and the corresponding one of a MOSFET are given by: $f_T(MOSFET)=\frac{g_m}{2\pi(C_{gs}+C_{gd})}, f_T(BJT)=\frac{g_m}{2\pi(C_\pi+C_\mu)}$. Does the **Miller effect** play an important role in the derivations of these two equations? (Please explain your answer based on Figure 3) (8 分)

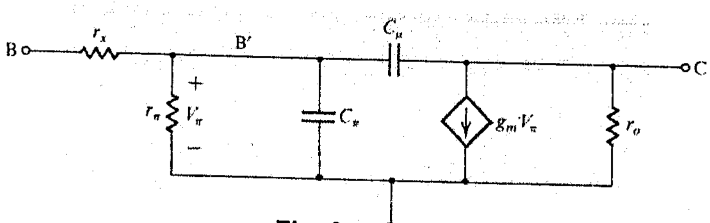

Fig. 3

注意：背面有試題

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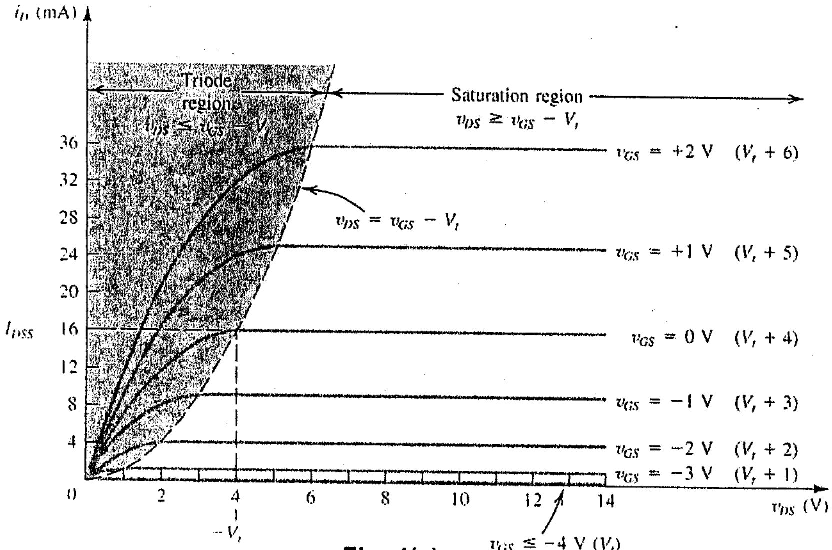

Fig. 4(a)

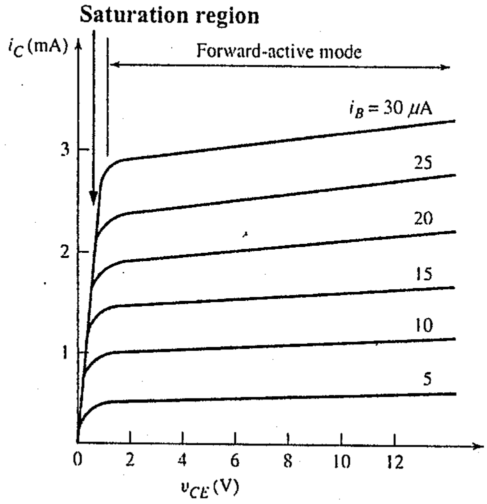

Fig. 4(b)

3. 簡答與選擇題 (12 分)

Figure 4 (a) and (b) shows the typical i_D - v_{DS} and i_C - v_{CE} curves of a MOSFET and an npn BJT.

3-1 Explain why the BJT amplifier usually has a better linearity than that of the MOSFET amplifier, based on these two typical *I*-*V* curves? (8 分)

3-2 In Fig. 4(b), if the BJT enters the saturation region, can you tell me the values of which two circuit elements as shown in Fig. 3 will change significantly? (a) r_π and g_m, (b) C_π and C_μ, (c) C_π and r_o, (d) C_μ and g_m. (4 分)

4. 計算題 (18 分)

Calculate the voltage gains (v_o/ v_i) for the following circuits:

4-1 Figure 5(a) shows a folded MOS amplifier formed by cascading two common source stages. Assuming Q_1 and Q_2 have the same transconductance of 1 mA/V, bias current I = 100 μA, $V_{An} = |V_{Ap}|$ = 2 V, and the biasing current sources have an output resistance equal to that of Q_1. Find its overall voltage gain. (6 分)

4-2 The MOSFETs in the circuit of Fig. 5(b) are matched, having $\mu_n C_{ox} (W/L)_1 = \mu_p C_{ox}(W/L)_2$ = 1.0 mA/V^2, threshold voltage $|V_t|$ = 0.5 V, $r_O = \infty$, and feedback resistor R_F = 100 kΩ . Find the voltage gain of the amplifier. (6 分)

4-3 Figure 5(c) shows a circuit for a voltage to current converter employing an op-amp with an open circuit voltage gain A = 1000. The MOSFET Q_1 has a transconductance g_m = 1.0 mA/V and $r_O = \infty$, a source resistor R_S = 1 kΩ and a drain resistor R_D = 10 kΩ. Find its closed-loop voltage gain. (6 分)

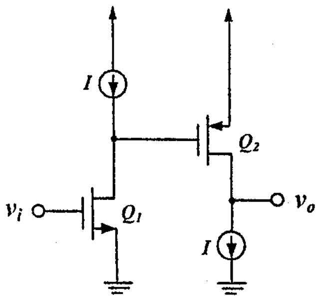

Fig. 5(a)

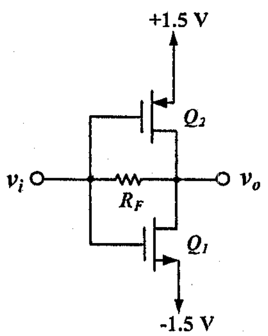

Fig. 5(b)

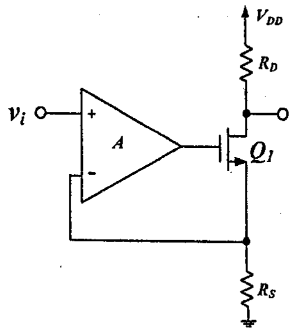

Fig. 5(c)

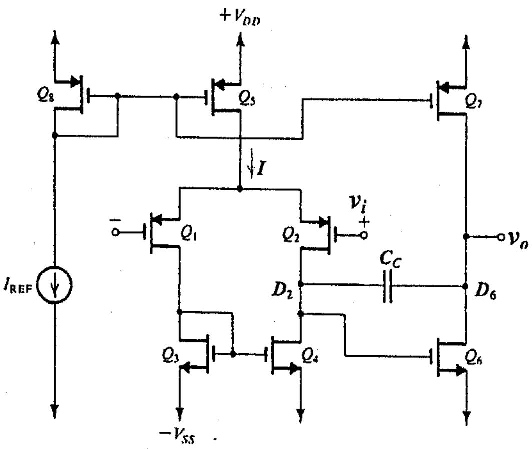

Fig. 6

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5. 計算題 (18 分)

Figure 6 shows the topology of a two-stage CMOS operational amplifier. The design parameters are listed as follows: $(W/L)_1 = (W/L)_2 = 20\ \mu m/0.8\ \mu m$, $(W/L)_3 = (W/L)_4 = 5\ \mu m/0.8\ \mu m$, $(W/L)_6 = 10\ \mu m/0.8\ \mu m$, $(W/L)_5 = (W/L)_7 = (W/L)_8 = 40\ \mu m/0.8\ \mu m$, $I_{REF} = 90\ \mu A$, $V_{tn} = 0.7$ V, $V_{tp} = -0.8$ V, $\mu_n C_{ox} = 160\ \mu A/V^2$, $\mu_p C_{ox} = 40\ \mu A/V^2$, $|V_A| = 9$ V for all devices, $V_{DD} = V_{SS} = 2.5$ V. The total capacitance between node D_2 and ground is $C_1 = 0.1$ pF, and the total capacitance between the output and ground is $C_2 = 2$ pF.

5-1 Find the dc open-loop voltage gain. (6 分)

5-2 Find the value of C_C that results in an unit-gain frequency $f_t = 10$ MHz. And also find the corresponding frequencies of transmission zero f_Z and second pole f_{p2}. (6 分)

5-3 If a resistor R is placed in series with C_C, find the value of R to obtain the transmission zero to be located at infinite frequency. (6 分)

6. 計算題 (16 分)

The circuit shown in Fig. 7 is a CMOS clocked SR flip-flop. The clock signal is denoted by ϕ. This circuit is fabricated in a process technology for which $\mu_n C_{ox} = 2.5\ \mu_p C_{ox} = 100\ \mu A/V^2$, $V_{tn} = |V_{tp}| = 1$ V, and $V_{DD} = 5$ V. The inverters have $(W/L)_n = 6\ \mu m/3\ \mu m$, $(W/L)_p = 15\ \mu m/3\ \mu m$. The four NMOSFETs in the set-reset circuit have equal W/L ratios.

6-1 Estimate the required minimum value for this ratio to ensure that the flip-flop will switch. (8 分)

6-2 Repeat to estimate the minimum required $(W/L)_5 = (W/L)_6$ so that the switching is achieved when inputs S and ϕ are at $V_{DD}/2$.(8 分)

7. 計算題 (14 分)

The circuit shown in Fig. 8 is a phase-shifter with an ideal op-amplifier.

7-1 Find the transfer function $T(s)$ and the corresponding pole and zero, (6 分)

7-2 What is the phase shift at transfer-function zero? (4 分)

7-3 For an input frequency of 10^4 Hz, and $C = 1.59$ nF, what value of R is required for phase-shift magnitude of 120° ? (4 分)

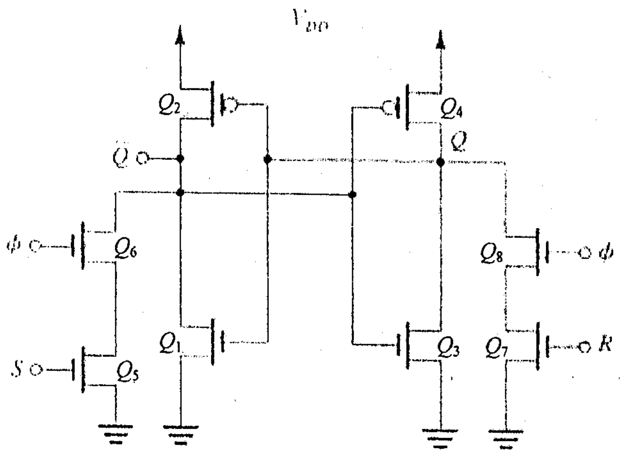

Fig. 7

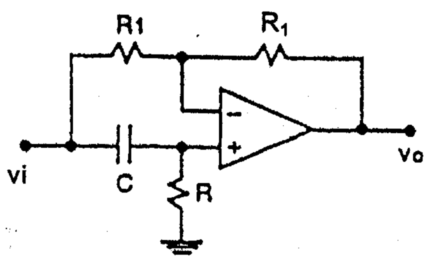

Fig. 8